ABSTRACT

A programmable input voltage range analog-to-digital converter in which a split gate oxide process allows the use of high voltage (±15 volt) switches on the same silicon substrate as standard sub-micron 5 volt CMOS devices. With this process, the analog input voltage can be sampled directly onto one or more sampling capacitors without the need for prior attenuation circuits. By only sampling on a given ratio of the sampling capacitors, the analog input can be scaled or attenuated to suit the dynamic range of a subsequent ADC. In the system of the present invention, the sampling capacitor can be the actual capacitive redistribution digital-to-analog converter (CapDAC) used in a SAR ADC itself, or a separate capacitor array. By selecting which bits of the CapDAC or separate sampling array to sample on, one can program the input range. Once the analog input signal has been attenuated to match the allowed dynamic range of the SAR converter, traditional SAR techniques can be used to convert the input signal to a digital word. Other conversion technologies, such as sigma-delta and pipeline, can also be used in conjunction with the inventive system.